

GA-E350N-USB3

OCT.20, 2010

Revision : 1.02

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	APU DDRIII, PCI_E
05	APU CONTROL
06	APU POWER & GND
07	DDRIII CHANNEL A
08	RTM880T-792/S
09	HUDSON PCIE/PCI/CPU/LPC/CLK
10	HUDSON ACPI/GPIO/USB/AUDIO
11	HUDSON SATA/IDE/HWM/SPI
12	HUDSON POWER & GND
13	PCI_E x4, VGA
14	HDMI ,DVI
15	ITE 8720 JX
16	ALC892 CODEC
17	AUDIO JACK
18	F_USB, FAN, HWMO
19	POWER SEQUENCE ,EUP
20	VCORE (PWMISL6329+6612)
21	SB, APU18 V, APU10V, VCC11_DUAL POWER
22	DDR POWER , VCC18
23	LAN RTL8111E
24	NEC USB3 uP720200
25	

GIGABYTE™			
Title COVER SHEET			
Size	Document Number		Rev
Custom	GA-E350N-USB3		1.02
Date:	Tuesday, January 25, 2011	Sheet	1 of 24

Model Name:GA-E350N-USB3

Component value change history

Version: 1.02

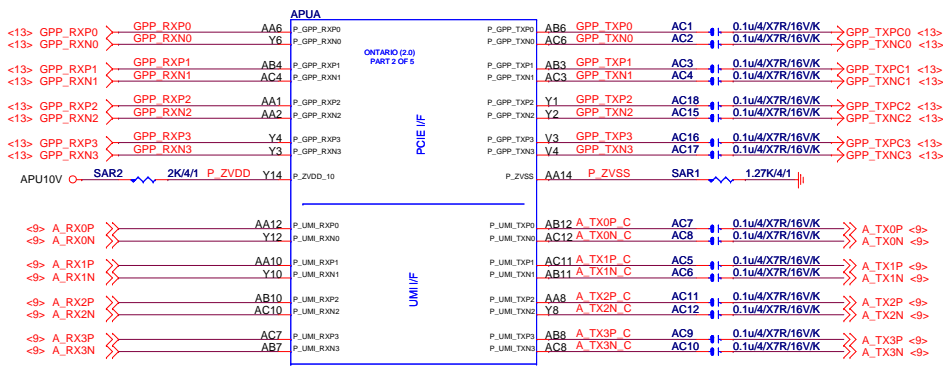
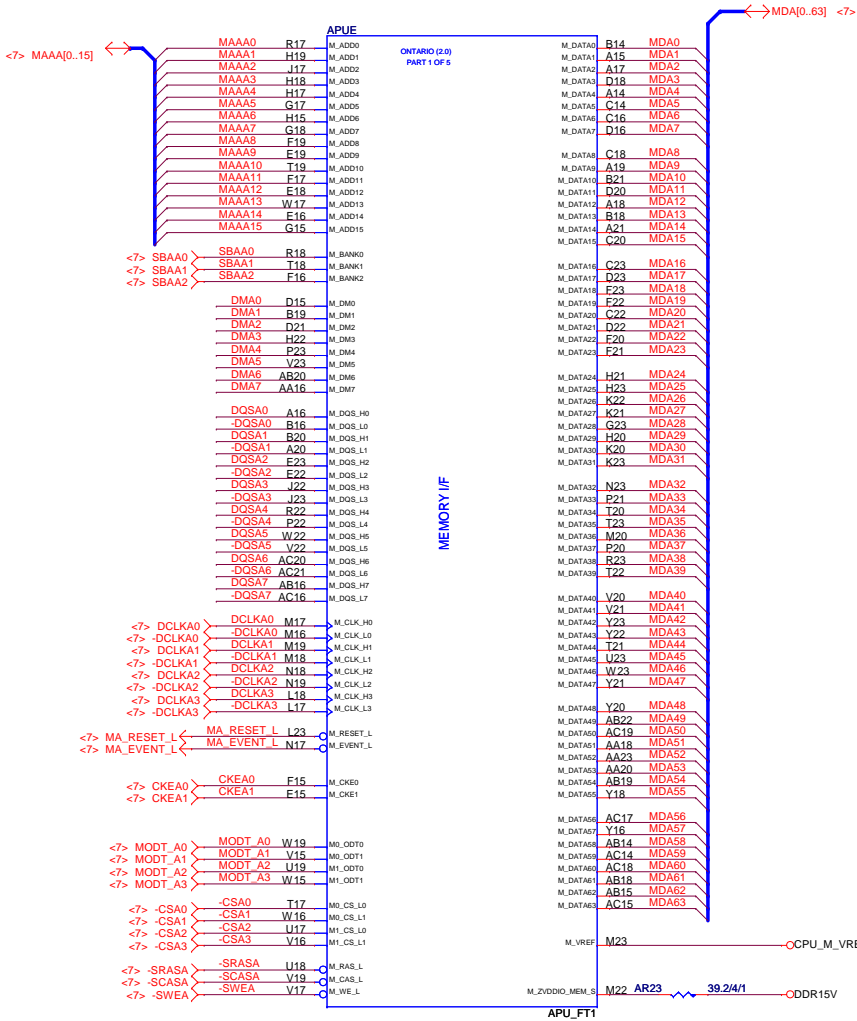
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[illegible]

Circuit or PCB layout change for next version

[illegible]

The diagram illustrates the system architecture of the RTM880T-792. At the top center is the **APU FT1** (4,5,6) with a **DX11 IGP**. It is connected to **UNBUFFERED DDRIII DIMM1** (7) and **UNBUFFERED DDRIII DIMM2** (7) via **DDRIII 1066,1333** (64bit) and **DDRIII FIRST LOGICAL DIMM** / **DDRIII SECOND LOGICAL DIMM**. Below the APU is the **HUDSON-M1** (16,17,18,19) which includes **USB2.0**, **SATA III**, **AZALIA**, **ACPI**, **LPC I/F**, and **INT RTC**. It is connected to the APU via a **Unified Media Interface** (4 x1) and **OUT** / **IN** signals. The Hudson-M1 is connected to various peripherals: **ALC892 HD AUDIO CODEC** (16,17) via **HD AUDIO I/F**, **SATA#0** (11), **SATA#1** (11), **SATA#2** (11), and **SATA#3** (11) via **SATA III I/F**, **SPI Dual-BIOS** (11) via **SPI I/F**, and **ITE LPC SIO IT8720** (15) via **LPC BUS**. The ITE LPC SIO IT8720 is connected to **KB_MS** (15) and **HW MONITOR** (15) via **SB_SPI_CS** and **ITE_SPI_CS1/2**. The Hudson-M1 is also connected to **NEC USB3 uP720200A** (24) and **GIGABIT RTL8111E** (23) via **1X PCIE INTERFACE**. It is connected to **USB-4** (15), **USB-3** (23), **USB-2** (23), **USB-1** (23), **USB-0** (23), **USB-5** (15), **USB-6** (18), and **USB-7** (18) via **USB 2.0**. The system is powered by **DESKTOP FT1 Power ISL6329** (20), **APUVDD18 & APU10 & VCC11_DUAL Power** (21), **DDR3 MEMORY POWER & DDRVTT 3VDUAL** (22), and **Hudson CORE POWER** (21). A **Clock Generator RTM880T-792** (8) is connected to **DVI** (14), **HDMI** (14), **VGA CON** (13), and **PCIE SLOT 4X** (13) via **TMD5/HDMI**, **TMD5/HDMI**, **RGB**, and **4X** signals.



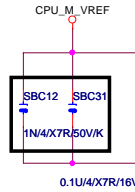
PCI E slot TX need CAP close to slot side
Ref to GND.

PLACE THESE CAP CLOSE TO APU
Ref to GND.

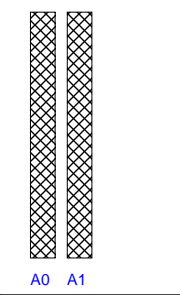


CPUVREF

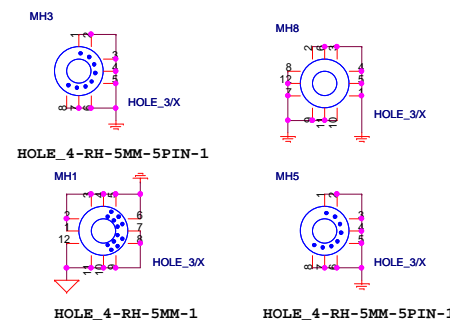
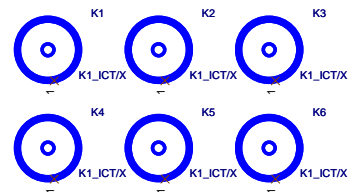
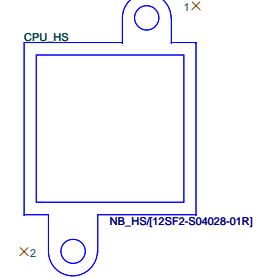
40 MILS WIDTH



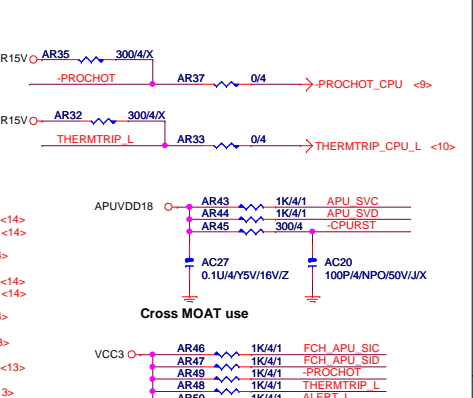
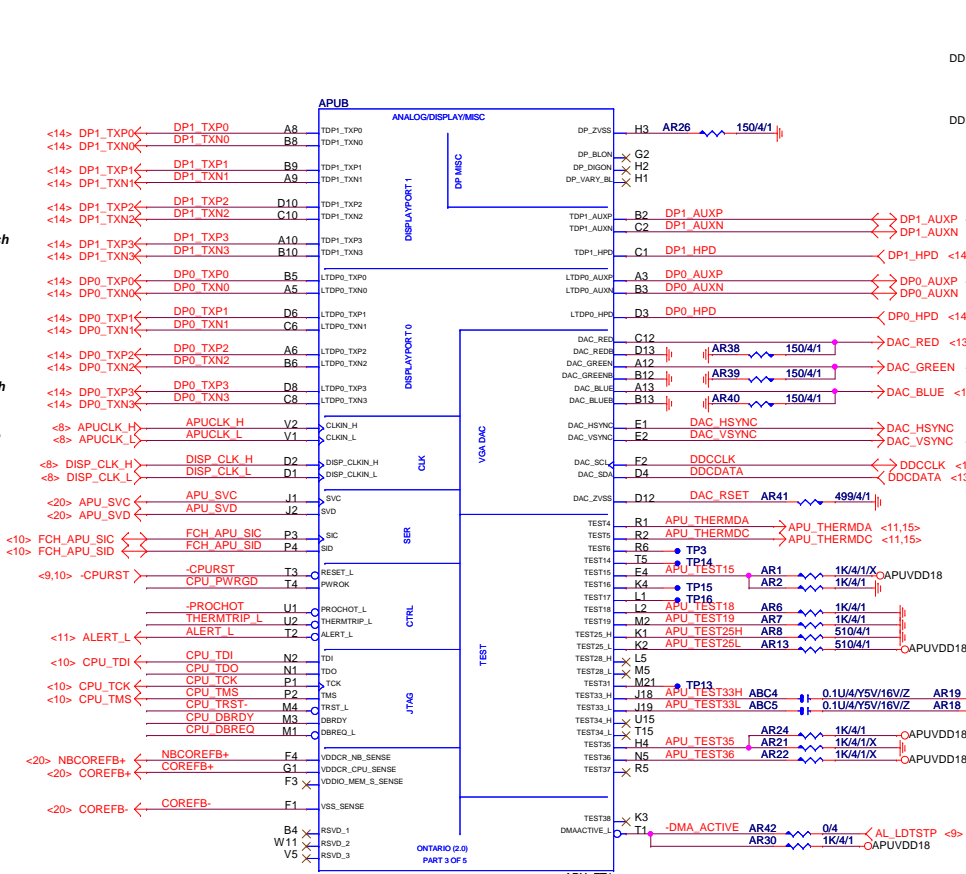
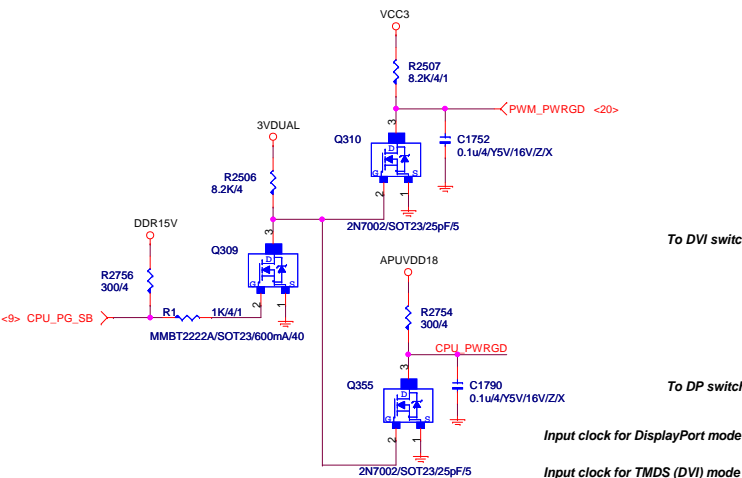
MEM CHA



NB_HEATSIN

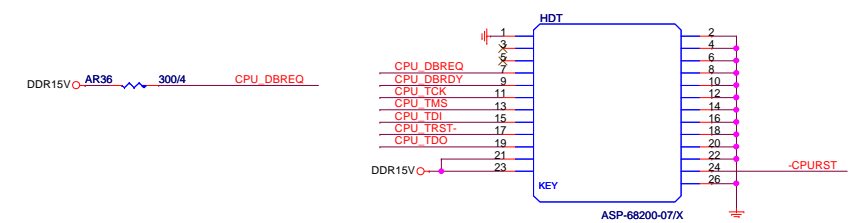


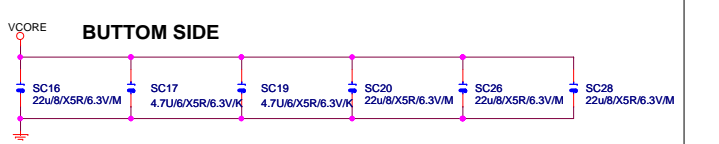
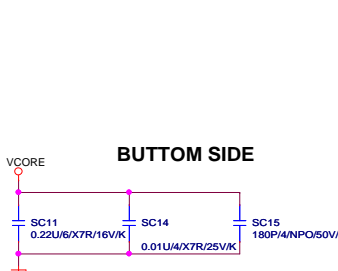
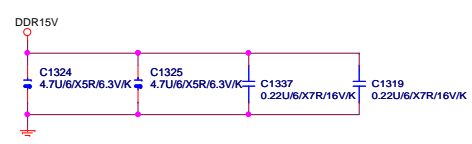
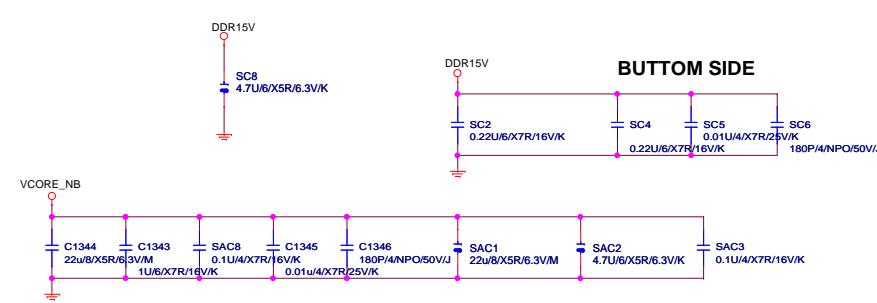
GIGABYTE		
Title		
COVER SHEET		
Size	Document Number	Rev
Custom	GA-E350N-USB3	1.02
Date:	Tuesday, January 25, 2011	Sheet 4 of 24

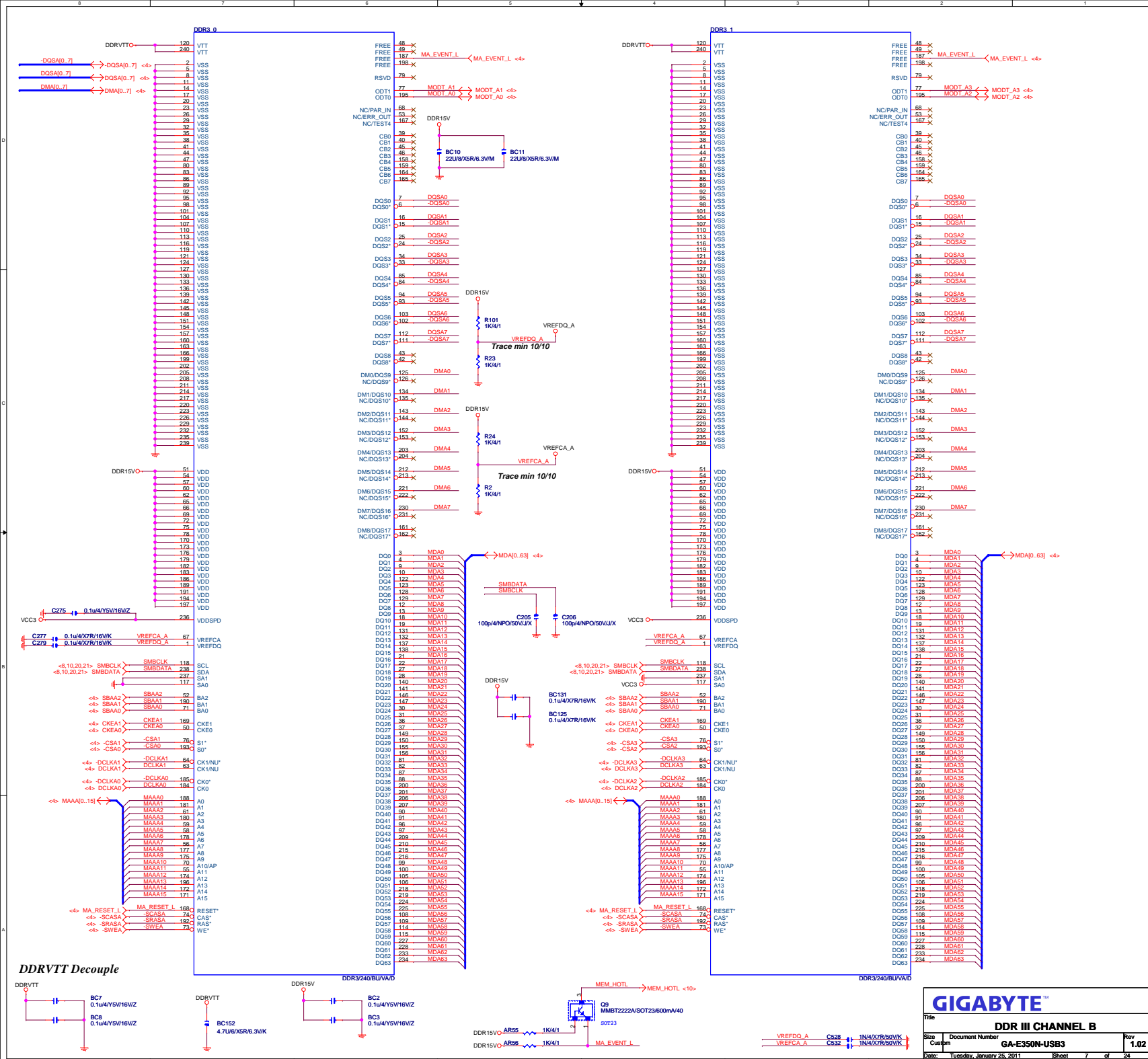


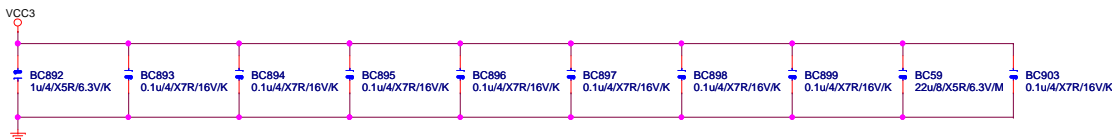
APU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
APU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B





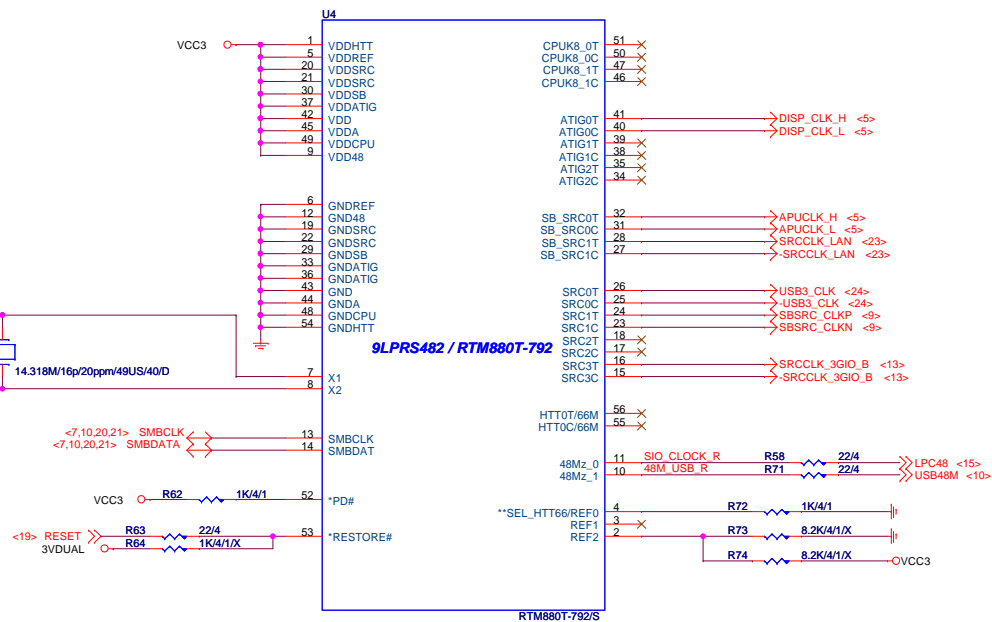




NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

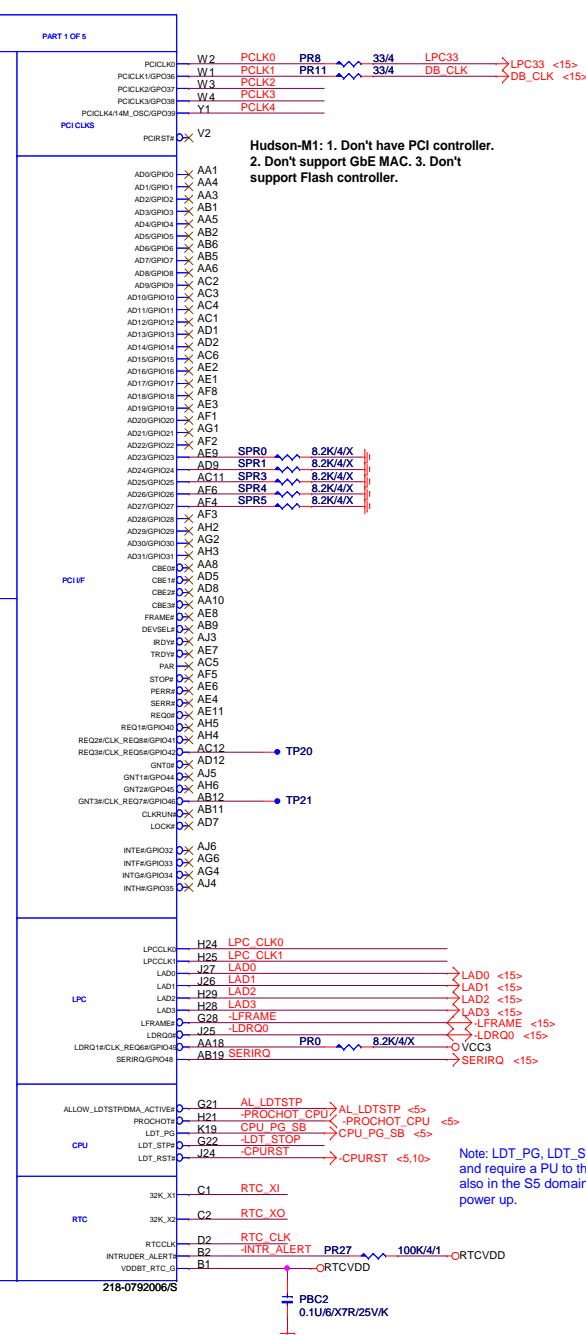
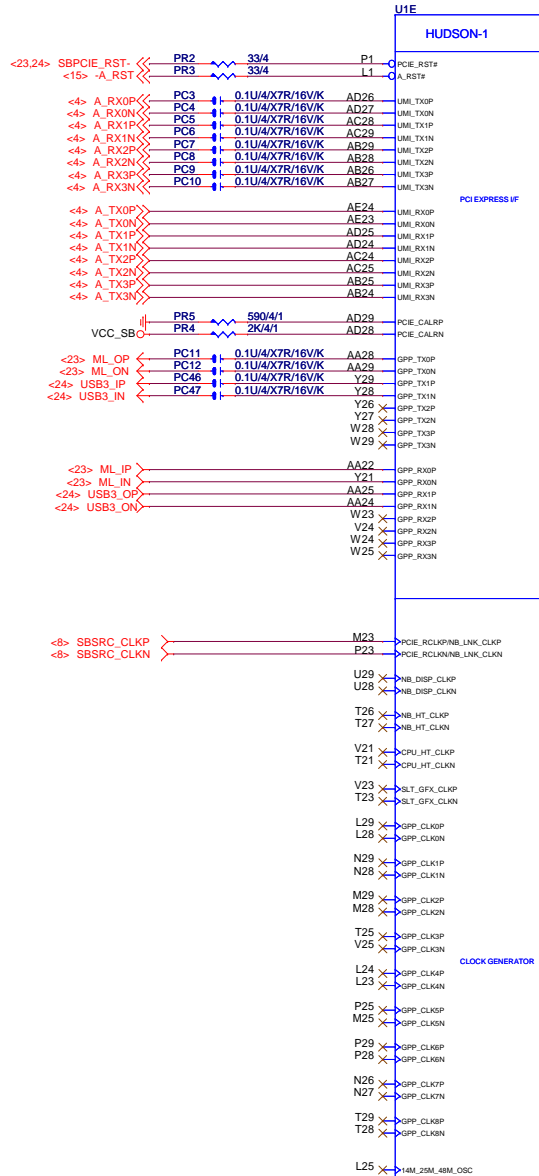
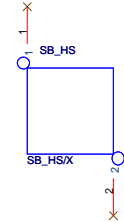
* the GFX_REFCLK input is required for all cases





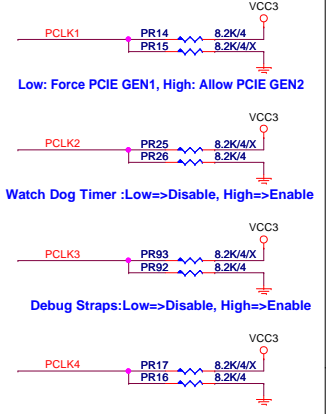
PLACE THESE PCIE AC COUPLING
CAPS CLOSE TO SB850

S.B HEATSINK

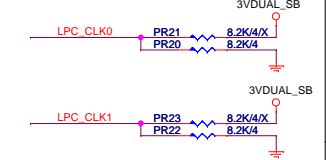


Hudson-M1: 1. Don't have PCI controller.
2. Don't support GbE MAC. 3. Don't support Flash controller.

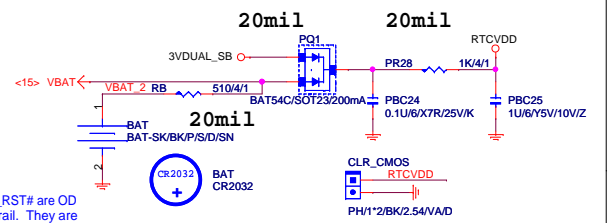
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.



Fusion clock mode :Low=>Enable, High=>Disable
This strap is not used if the strap CLKGEN is configured for external clock generator mode.



LPC_CLK0 LPC_CLK1
PULL HIGH IMC ENABLED Internal Clock Mode
PULL LOW IMC DISABLED External Clock Mode
DEFAULT DEFAULT



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

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TitleATI SB700 PCIE/PCI/CPU/LPC

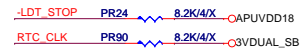
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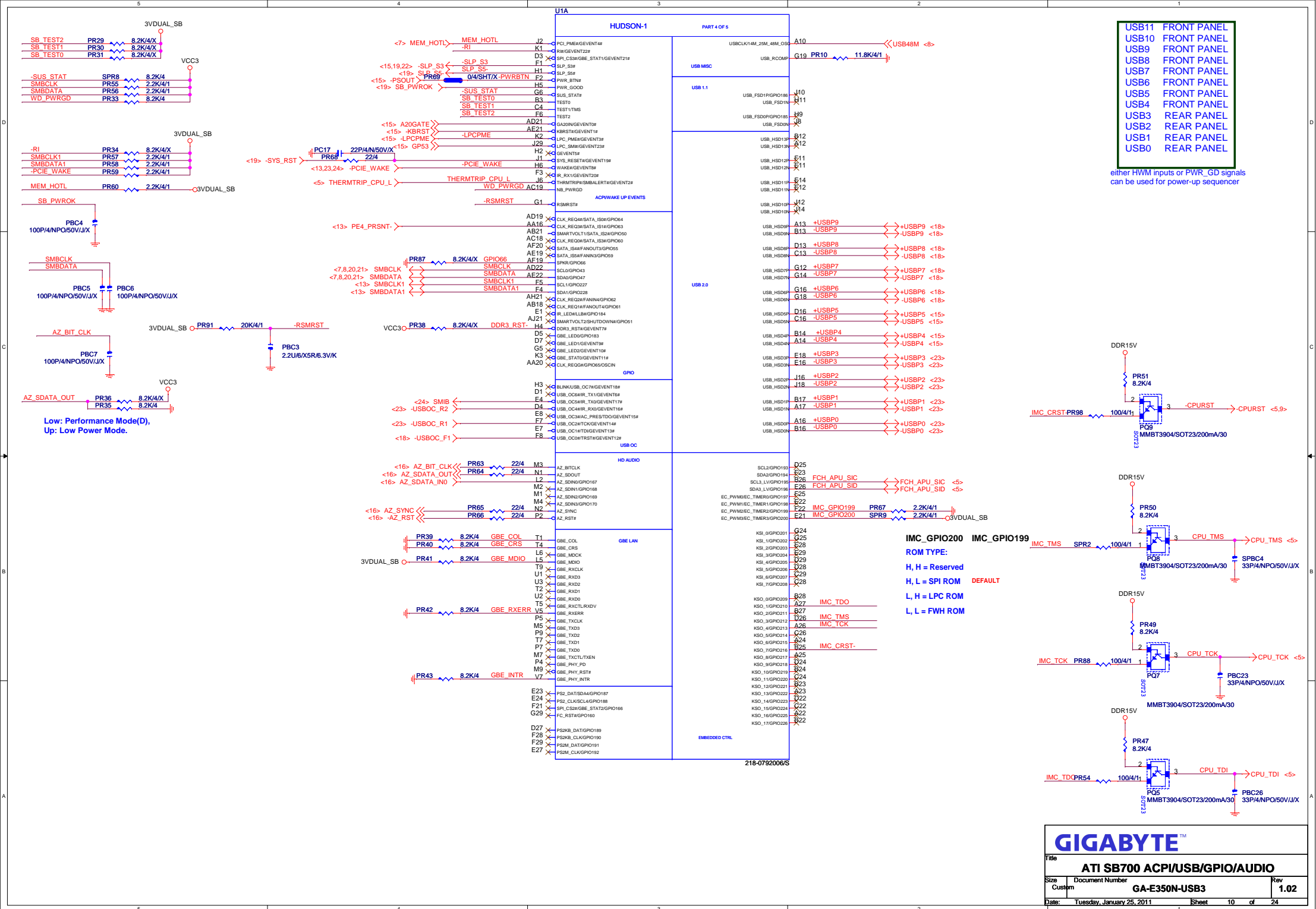
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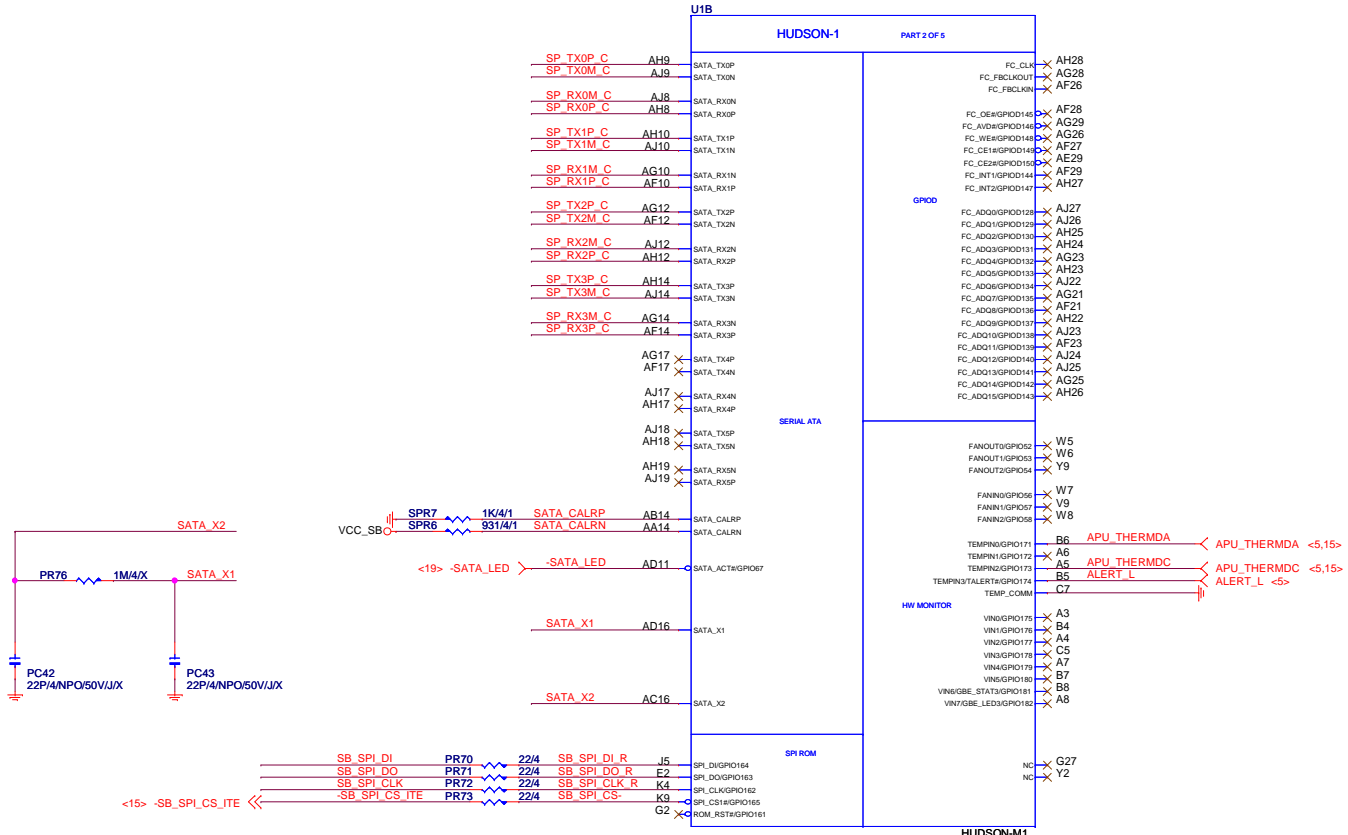
DateTuesday, January 25, 2011

Sheet9 of 24

Rev1.02

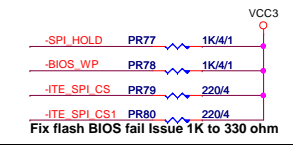
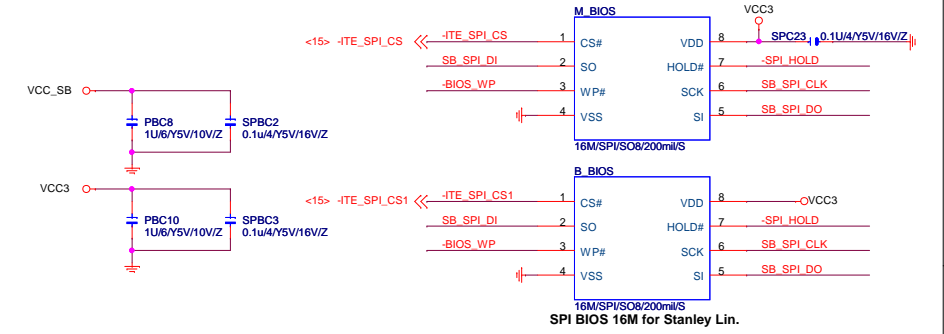
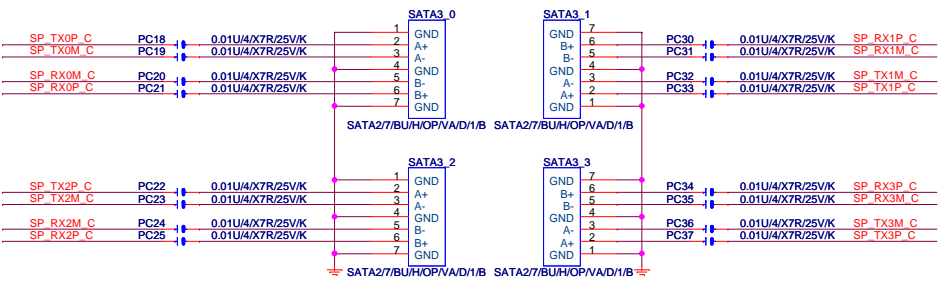






PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

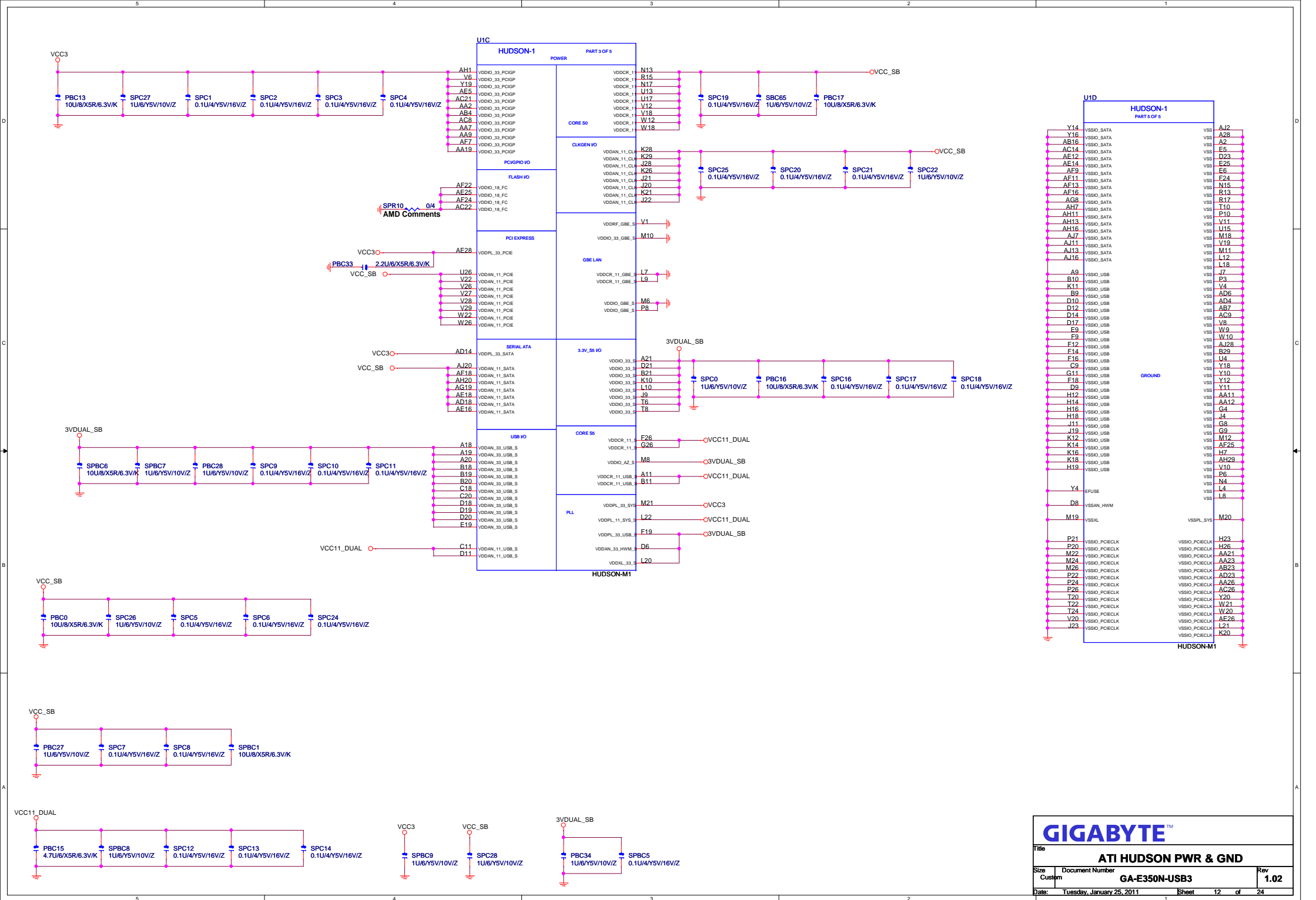


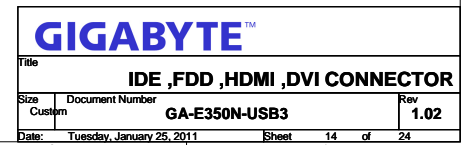
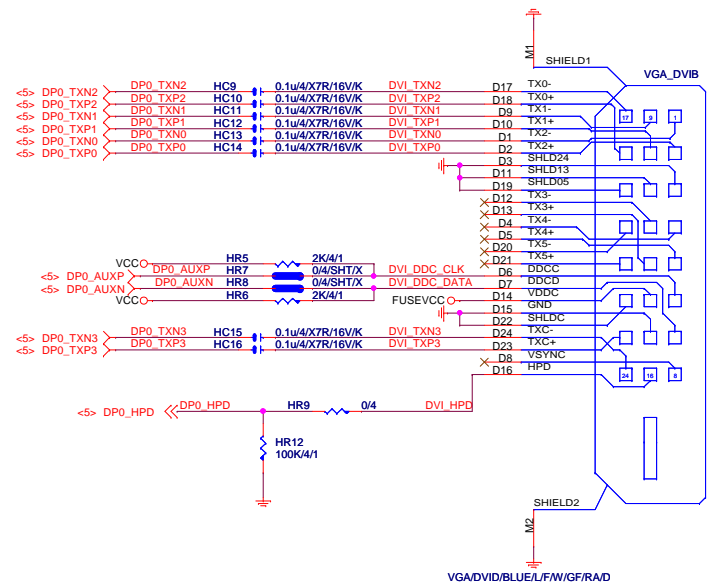
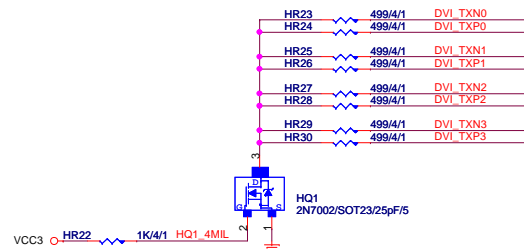
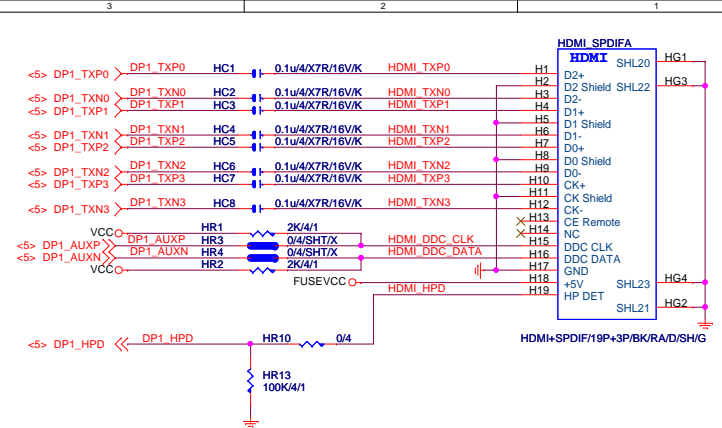
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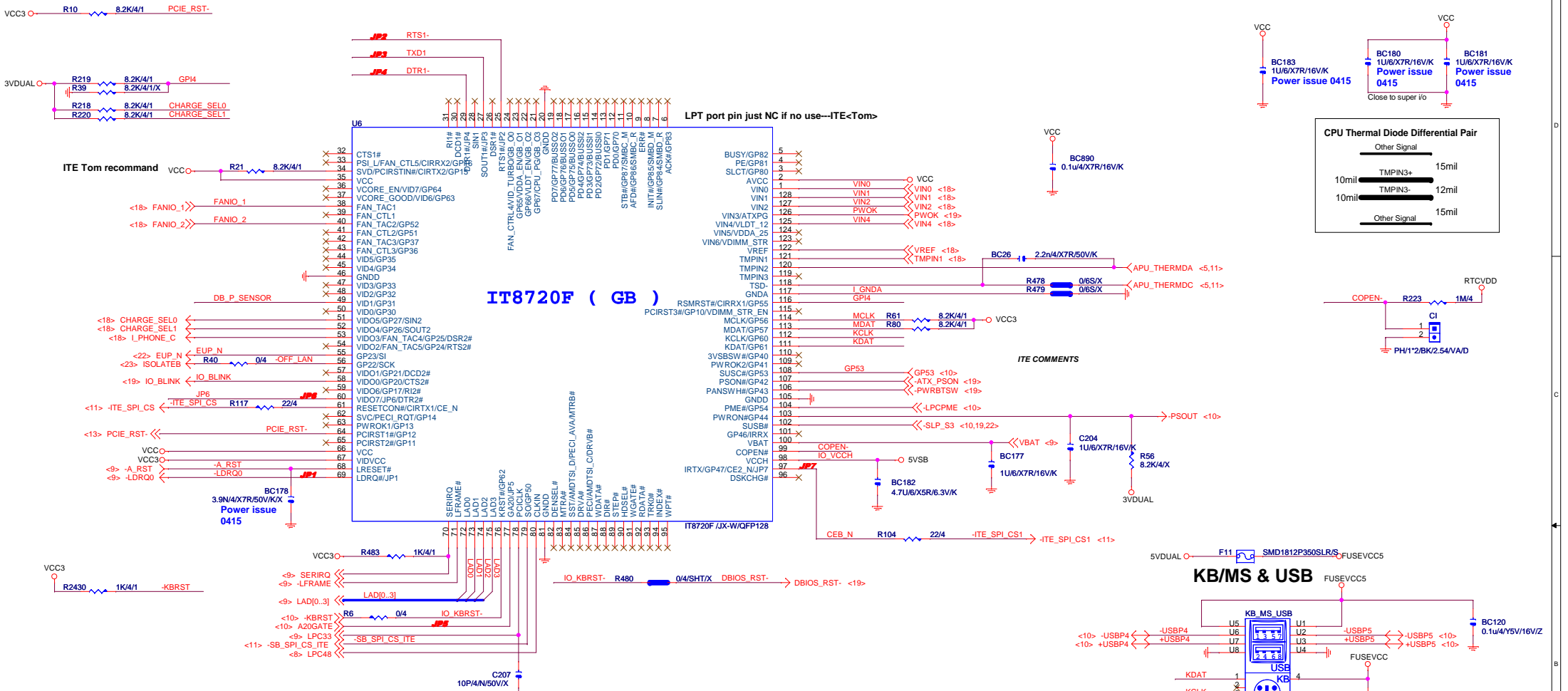
ATI SB700 SATA/IDE/HWM/SPI

Size Custom Document Number **GA-E350N-USB3** Rev **1.02**

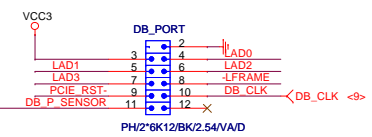
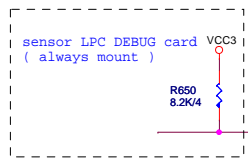
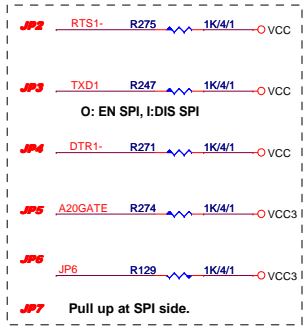
Date: Tuesday, January 25, 2011 Sheet 11 of 24







Symbol	value	Description
JP1		
Pin 69		
JP2	VIDO_EN	1 Disable VID output pins
Pin 25		0 Enable VID output pins
JP3	Flashseg1_EN	1 Disabled.
Pin 27		0 Flash I/F Address Segment 1 is enabled
JP4	K8PWR_EN	1 K8 power sequence disabled
Pin 29		0 K8 power sequence enabled
JP3 & JP5	FAN_CTL_SEL	11 Half Run Default value of EC Index 15h/16h/17h is 40h
Pin 27 & Pin 77		10 No Run Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run Default value of EC Index 15h/16h/17h is 00h
		00 75% Run Default value of EC Index 15h/16h/17h is 20h
JP5	WDT_EN	1 Disable WDT to rest PWROK
Pin 77		0 Enable WDT to rest PWROK
JP6	SVID_EN	1 Disable SVID Function
Pin 60		0 Enable SVID Function
JP7	Dual_BIOS_EN	1 Enable Dual BIOS Function for GigaByte Only
Pin 97		0 Disable Dual BIOS Function for GigaByte Only



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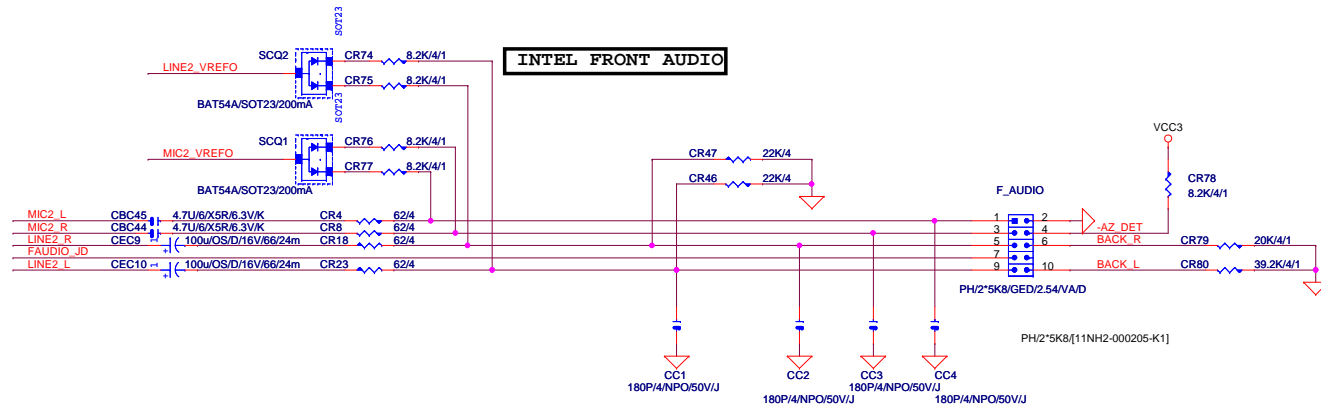
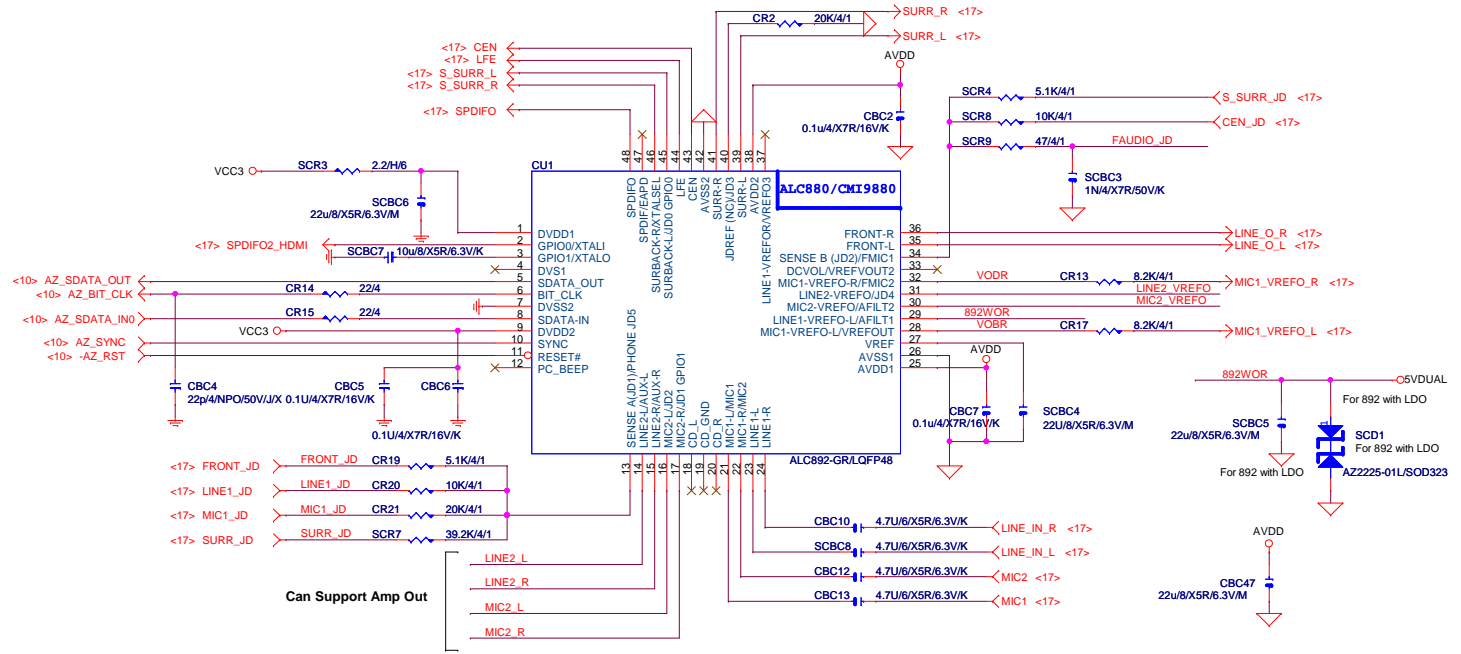
ITE 8720 LPC IO ,Dual-BIOS

Size	Document Number	Rev
Custom	GA-E350N-USB3	1.02

Date	Tuesday, January 25, 2011	Sheet	15	of	24
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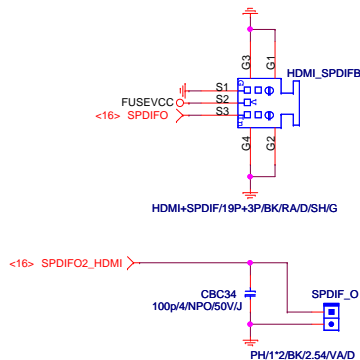
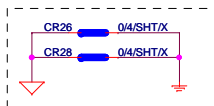
AZALIA CODEC ALC892/ALC889/ Colay

	ALC892	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm

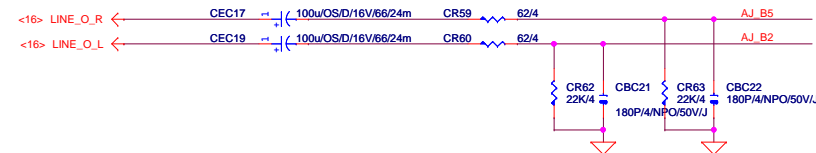


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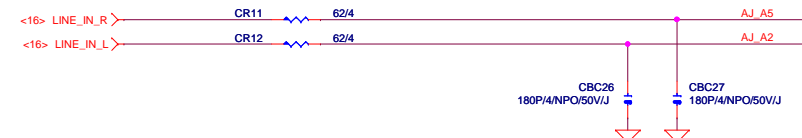
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Size	Document Number	Rev			
Custom	GA-E350N-USB3	1.02			
Date:	Tuesday, January 25, 2011	Sheet	16	of	24



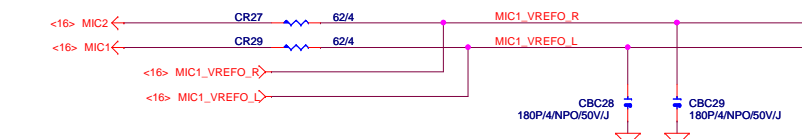
LINE OUT FRONT OUT



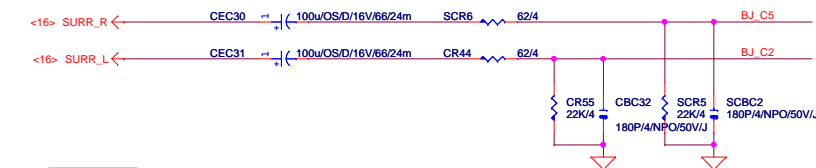
LINE-IN



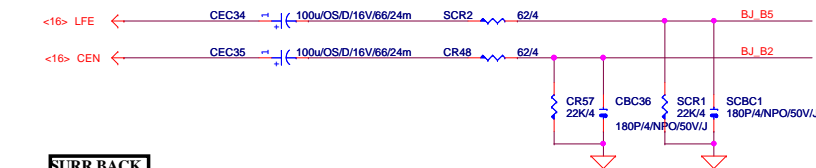
MIC



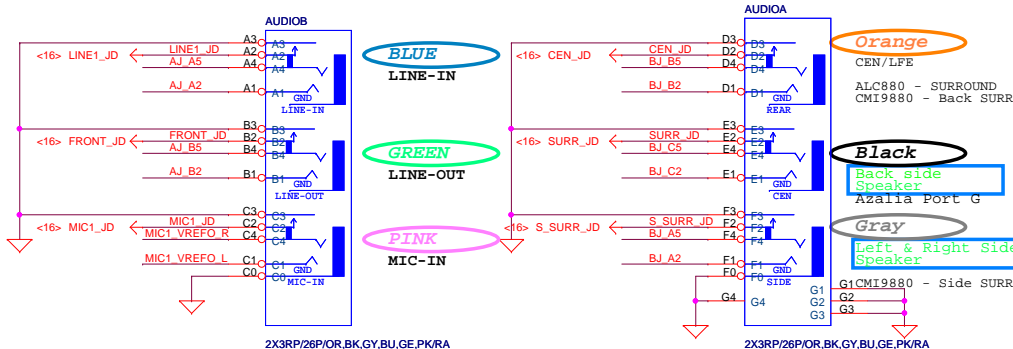
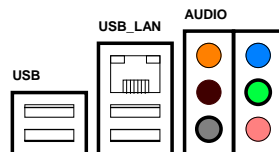
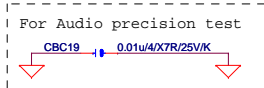
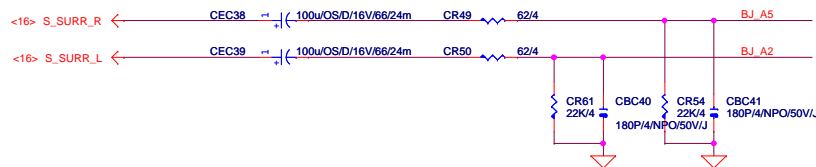
SURROUND



CEN/LFE



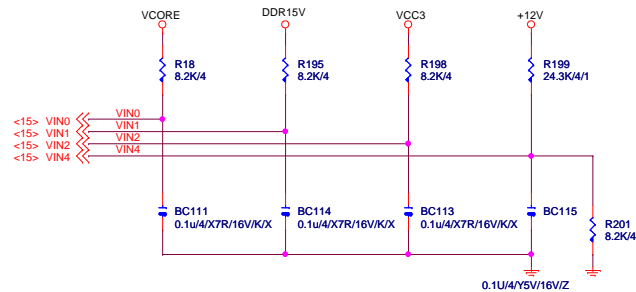
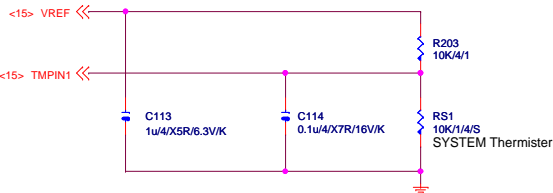
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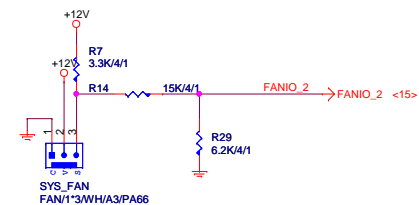
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Title			
AUDIO JACK			
Size	Document Number	Rev	
Custom	GA-E350N-USB3	1.02	
Date:	Tuesday, January 25, 2011	Sheet	17 of 24

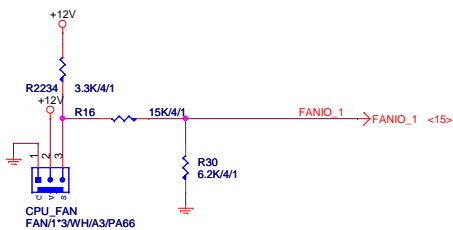
Hardware Monitor circuits



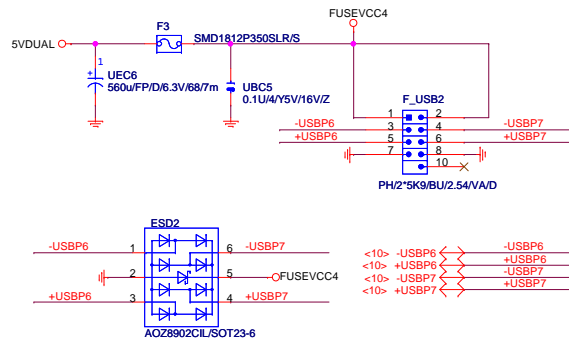
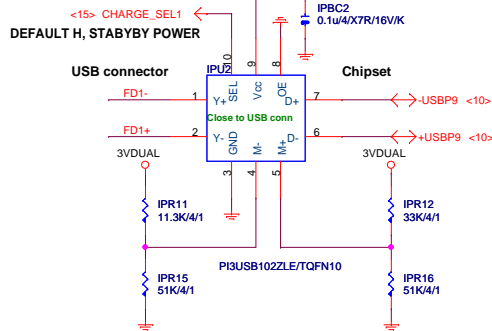
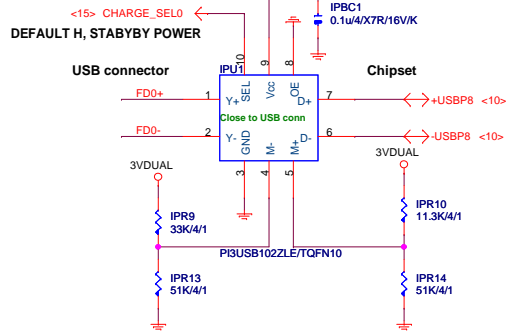
SYSTEM FAN



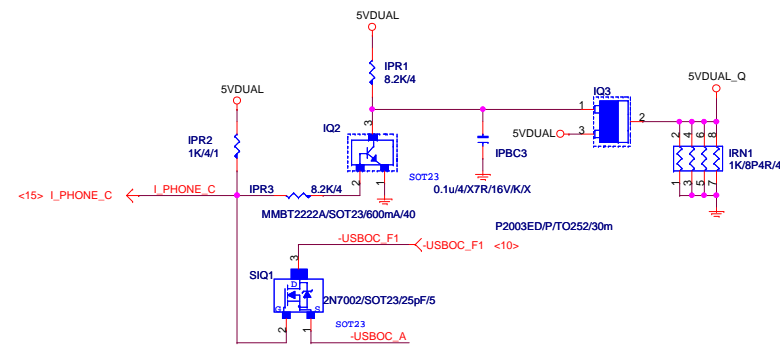
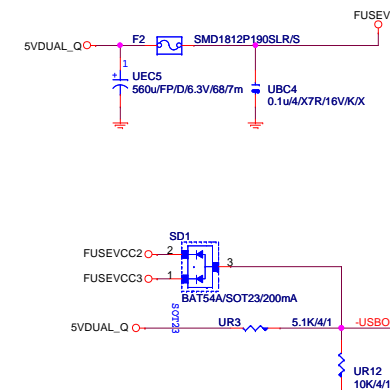
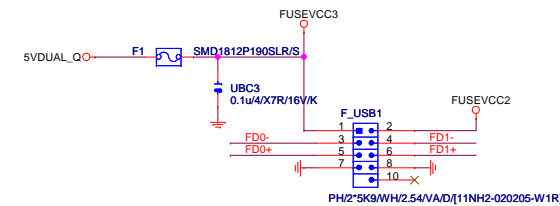
CPU FAN



i_Phone charger circuit



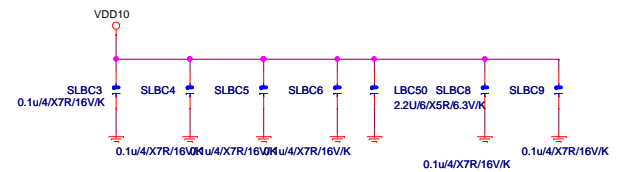
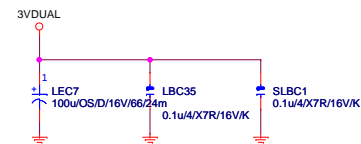
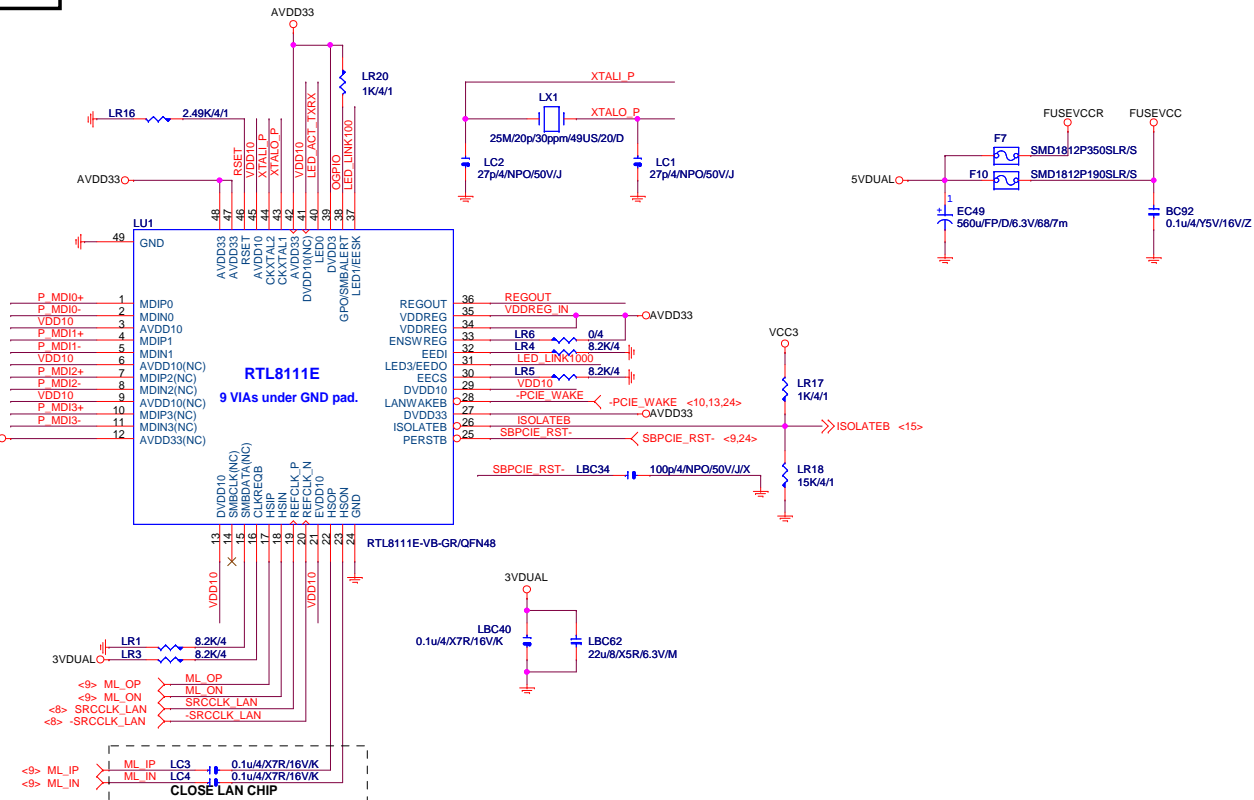
FRONT USB



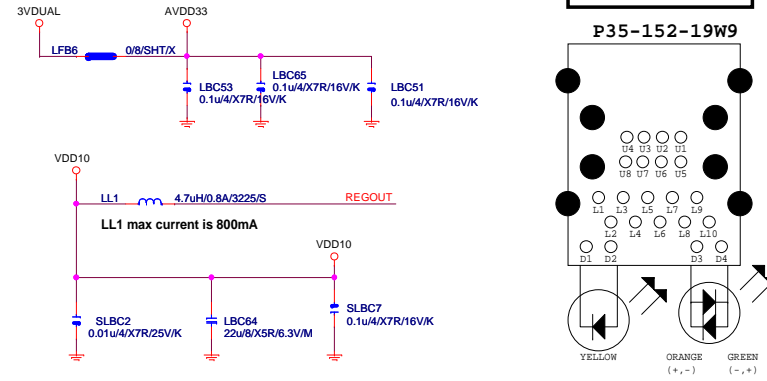
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Title			COM/F_USB
Size	Document Number	Rev	1.02
Custom	GA-E350N-USB3		
Date:	Tuesday, January 25, 2011	Sheet	18 of 24

PCIE-1G LAN



USB_LAN CONNECTOR



USB_LAN

